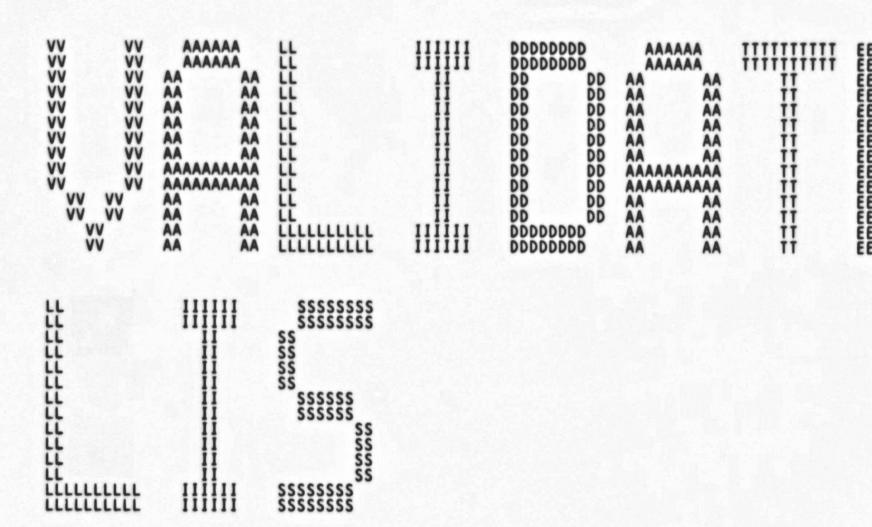
\$	DDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDD	AAAAAAA AAAAAAA AAAAAAA
\$\$\$ \$\$\$ \$\$\$ \$\$\$ \$\$\$ \$\$\$	DDD DDD DDD DDD	AAA AAA
SSS	DDD DDD	AAA AAA
\$\$\$\$\$\$\$\$\$ \$\$\$\$\$\$\$\$\$	DDD DDD DDD DDD	AAA AAA
SSSSSSSSS SSS SSS	DDD DDD DDD DDD	AAA AAAAAAAAAAAAA AAAAAAAAAAAA
\$\$\$ \$\$\$ \$\$\$	DDD DDD	AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA
\$\$\$ \$\$\$ \$\$\$	DDD DDD DDD DDD DDD DDD	AAA AAA
\$	DDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDD	AAA AAA



LIBS VO4

VALIDATE Table of contents

(1) 53 DECLARATIONS
(1) 81 VAL_SET_MAX - Set maximum number of links to traverse
(2) 122 VALIDATE_QUEUE - Validate queue structure

LIB VO4

LIB VO4

VALIDATE - Structure Validation module

COPYRIGHT (c) 1978, 1980, 1982, 1984 BY DIGITAL EQUIPMENT CORPORATION, MAYNARD, MASSACHUSETTS. ALL RIGHTS RESERVED.

THIS SOFTWARE IS FURNISHED UNDER A LICENSE AND MAY BE USED AND COPIED ONLY IN ACCORDANCE WITH THE TERMS OF SUCH LICENSE AND WITH THE INCLUSION OF THE ABOVE COPYRIGHT NOTICE. THIS SOFTWARE OR ANY OTHER COPIES THEREOF MAY NOT BE PROVIDED OR OTHERWISE MADE AVAILABLE TO ANY OTHER PERSON. NO TITLE TO AND OWNERSHIP OF THE SOFTWARE IS HEREBY TRANSFERRED.

THE INFORMATION IN THIS SOFTWARE IS SUBJECT TO CHANGE WITHOUT NOTICE AND SHOULD NOT BE CONSTRUED AS A COMMITMENT BY DIGITAL EQUIPMENT CORPORATION.

DIGITAL ASSUMES NO RESPONSIBILITY FOR THE USE OR RELIABILITY OF ITS SOFTWARE ON EQUIPMENT WHICH IS NOT SUPPLIED BY DIGITAL.

ABSTRACT:

This module contains code which verifies the consistency of certain VMS internal structues.

ENVIRONMENT:

VMS user mode.

AUTHOR: Jake VanNoy, CREATION DATE: 21-Jan-1983

MODIFIED BY:

V03-000 JLV0226 Initial coding. Jake VanNoy

21-JAN-1983

.SBTTL DECLARATIONS

INCLUDE FILES:

FACILITY:

SDA

VALIDATE
- Structure Validation module 16-SEP-1984 01:48:32 VAX/VMS Macro V04-00 Page 3 VAL_SET_MAX - Set maximum number of link 5-SEP-1984 03:34:48 [SDA.SRC]VALIDATE.MAR;1 (1) 0000 0004 115 Entry VAL_SET_MAX, 0 0006 117 F5 AF 1C AC DO 0006 118 MOVL TPA\$L_NUMBER(AP), VALIDATE_MAX ; set max 04 000E 120 RET

LIB VO4

LIBS

00000000'EF 50 10 5E 56 RO.R3 (RO), HEADFL (R2),#8 53 DO 50 MOVL init last pointer TRYMEM ; try memory at head of queue DO 08 A2 HEADFL (R2),R4 ; next address MOVL Loop through flinks

C A2 O4 A2 D1 O05f O05f			A2 53 54	5020 1563 558 560 553 560 560 560 560 560 560 560 560 560 560	E9 13 06 01 120 00 11	0039 0039 0049 0049 004F 0051 0057 005A 005B	179 180 181 182 183 184 185 188 189 190 191	20\$:	TRYMEM BLBC CMPL BEQL INCL CMPL BNEQ MOVL MOVL BRB	(R4), NEWFL(R2),#8 R0,mem_err newfl(R2), headfl(R2) 100\$ R6 R3, NEWBL(R2) bad_blink R4,R3 NEWFL(R2),R4 20\$	<pre>; try memory ; Error ; Same as listhead? ; Done with flinks ; Increment counter ; back link ok? ; branch if not ; save last pointer ; move to next element ; Loop</pre>	
Oc A2 25 12 0064 194 BNEQ bad_blink							F 191 : Search completed successfully, do final validation					
198	00			A2 2F 53 29	D1 12 D1 12	005F 0064 0066 006A	194	100\$:	BNEQ CMPL	NEWBL(R2), HEADBL(R2) bad_blink R3, READBL(R2) bad_blink	; Done with list	
56 D5 006C 200 110\$: TSTL R6 BNEQ queue_ok 0070 202 PRINT 0, Queue_ok 0080 204 0080 204 0080 205 0080 206 0082 207 0082 207 0095 209 0095 210 0095 210 0097 212 0097 213 0097 213 0097 213 0097 214 0097 215 0097 215 0097 217 0097 217 0097 218 0097 219 0098 210 0099 210 0099 210 0099 211 0097 212 0097 213 0097 213 0097 213 0097 214 0097 215 0097 215 0097 216 0098 217 0098 217 0008 217 0008 217 0008 217 0008 217 0008 217 0008 217 0008 217 0008 217 0008 217 0008 217 0008 217 0008 217 0008 217 0008 217 0008 217 0008 217 0008 218 0008 219 0008 219 0008 219 0008 219 0008 219 0008 219 0008 219 0008 219 0008 219 0008 220 queue_ok: 0008 221 0008 221 0008 221 0008 221 0008 221 0008 221 0008 221 0008 221 0008 221 0008 221 0008 221 0008 221 0008 221 0008 221 0008 222 0006 223 0006 224 0006 225 0066 224 0060 226						0060	198		: Queue	is ok, check for empty	queue	
## 12 006E 201				56	D5		199	110\$:	İSTL	R6		
04 0094 208				47	12	006E	201		BNEQ	queue_ok		
04 0094 208			0	046	31	007D	203			VAL_Q_EXIT		
04 0094 208						0080	204	776 MAM				
0095 210 bad_blink: 53 DD 0095 211 PUSHL R3				54		0080 0082 0094	206 207 208	mem_err	SIGNAL		; Not in physical memory error	
DD 0095 211 PUSHL R3						0095						
00A8 216 PRINT 2,- 00A8 217 <error !ul="" !xl,="" address="" after="" at="" element="" element!%s="" in="" occured="" queue="" tracing=""> 0F 11 00B5 218 brb val_q_exit 00B7 219 00B7 220 queue_ok: 56 DD 00B7 221 PUSHL R6 00C6 223 00C6 223 00C6 224 val_q_exit: 00C6 225 00C6 225 00C6 225 00C6 227 00CA 227</error>				53	DD	0095	211		PUSHL			
00A8 216 PRINT 2,- 00A8 217 <error !ul="" !xl,="" address="" after="" at="" element="" element!%s="" in="" occured="" queue="" tracing=""> 0F 11 00B5 218 brb val_q_exit 00B7 219 00B7 220 queue_ok: 56 DD 00B7 221 PUSHL R6 00C6 223 00C6 223 00C6 224 val_q_exit: 00C6 225 00C6 225 00C6 225 00C6 227 00CA 227</error>				54	00		213	<error< td=""><td>comparing</td><td>backward link to previ</td><td>ous structure address (!XL)></td></error<>	comparing	backward link to previ	ous structure address (!XL)>	
00A8 216				54	DD	00A6	215		PUSHL	R4		
OF 11 00B5 218 brb val_q_exit 00B7 219 00B7 220 queue_ok: 56 DD 00B7 221 PUSHL R6 00B9 222 PRINT 1, <queue !ul="" complete,="" element!%s="" in="" is="" of="" queue="" the="" total=""> 00C6 223 00C6 224 val_q_exit: 50 01 D0 00C6 225 MOVL #1,R0 04 00C9 226 RET 00CA 227</queue>						8A00	216	/Error	PRINT	2,-	acc IVI after tracing IIII element IVC	
0087 220 queue_ok: 56 DD 0087 221 PUSHL R6 0089 222 PRINT 1, <queue !ul="" complete,="" element!%s="" in="" is="" of="" queue="" the="" total=""> 0006 224 val_q_exit: 50 01 D0 0006 225 MOVL #1,R0 04 0009 226 RET 000A 227</queue>				OF	11	0085	218	VETTOT (brb	val_q_exit	ess .AL, after tracing .OL etement. 237	
00B9 222 PRINT 1, <queue !ul="" complete,="" element!%s="" in="" is="" of="" queue="" the="" total=""> 00C6 223 00C6 224 val_q_exit: 50 01 D0 00C6 225 MOVL #1,R0 04 00C9 226 RET 00CA 227</queue>						00B7	219	queue of				
50 01 D0 00C6 225 MOVL #1,R0 04 00C9 226 RET 00CA 227 00CA 228 .END ; VALIDATE				56	DD	00B7 00B9	222	dacac_o	PUSHL	R6 1, <queue complete,<="" is="" td=""><td>; Count total of !UL element!%S in the queue></td></queue>	; Count total of !UL element!%S in the queue>	
00CA 227 00CA 228 .END ; VALIDATE			50	01	D0 04	00C6 00C6 00C9	224	val_q_e	MOVL RET	#1,R0		
						00CA 00CA	227	.END	;	VALIDATE		

LIB VO4

LIB VO4

The working set limit was 1050 pages.
13151 bytes (26 pages) of virtual memory were used to buffer the intermediate code.
There were 10 pages of symbol table space allocated to hold 182 non-local and 8 local symbols.
228 source lines were read in Pass 1, producing 21 object records in Pass 2.
13 pages of virtual memory were used to define 12 macros.

0 9 VALIDATE VAX-11 Macro Run Statistics Page 16-SEP-1984 01:48:32 VAX/VMS Macro V04-00 5-SEP-1984 03:34:48 [SDA.SRC]VALIDATE.MAR;1 - Structure Validation module (2) Macro library statistics ! Macros defined Macro library name _\$255\$DUA28:[SDA.OBJ]SDALIB.MLB;1 _\$255\$DUA28:[SYS.OBJ]LIB.MLB;1 _\$255\$DUA28:[SYSLIB]STARLET.MLB;2 TOTALS (all libraries) 040 275 GETS were required to define 9 macros. There were no errors, warnings or information messages. MACRO/LIS=LIS\$: VALIDATE/OBJ=OBJ\$: VALIDATE MSRC\$: VALIDATE/UPDATE=(ENH\$: VALIDATE) + EXECML\$/LIB+LIB\$: SDALIB/LIB

0354 AH-BT13A-SE

DIGITAL EQUIPMENT CORPORATION CONFIDENTIAL AND PROPRIETARY

